SECAB
Institute of Engineering and Technology,
Vijayapura

Approved by AICTE New Delhi, Recognized by Govt. of Karnataka and Affiliated to VTU Belgaum.

LABORATORY MANUAL

Semester: III

Course: Analog Electronic Circuits

Course Code: BEE303

Department of Electrical & Electronics Engineering

General Instructions

1. After circuit connection, before switching ON the supply, verify it by instructor or lab in charge.
2. Make sure voltage level of power supply is at minimum value at the start.
3. Before leaving the lab keep all the equipment's properly.

List of Experiments

Expt No.	Title of the Experiment
1	Experiments on series, shunt and double ended clippers and clampers.
2	Design, simulation and Testing of Full wave – centre tapped transformer type and Bridge type rectifier circuits with and without Capacitor filter. Determination of ripple factor, regulation and efficiency.
3	Static Transistor characteristics for CE, CB and CC modes and determination of h parameters.
4	Frequency response of single stage BJT and FET RC coupled amplifier and determination of half power points, bandwidth, input and output impedances.
5	Design and testing of BJT -RC phase shift oscillator for given frequency of oscillation.
6	Design, simulation (MATLAB) and testing of Wien bridge oscillator for given frequency of oscillation.
7	Design and testing of Hartley and Colpitt's oscillator for given frequency of oscillation.
8	Determination of gain, input and output impedance of BJT Darlington emitter follower with and without bootstrapping.
9	Design and testing of Class A and Class B power amplifier and to determine conversion efficiency.
10	Design and simulation of Full wave – centre tapped transformer type and Bridge type rectifier circuits with and without Capacitor filter using MATLAB. Determination of ripple factor, regulation and efficiency.

Evaluation Scheme

- **15 marks** for the conduction of the experiment and preparation of laboratory record, and **10 marks** for the test to be conducted after the completion of all the laboratory sessions.
- On completion of every experiment/program in the laboratory, the students shall be evaluated including viva-voce and marks shall be awarded on the same day.
- The CIE marks awarded in the case of the Practical component shall be based on the continuous evaluation of the laboratory report. Each experiment report can be evaluated for 10 marks. Marks of all experiments' write-ups are added and scaled down to **15 marks**.
- The laboratory test **(duration 02/03 hours)** after completion of all the experiments shall be conducted for 50 marks and scaled down to **10 marks.**
- Scaled-down marks of write-up evaluations and tests added will be CIE marks for the laboratory component of IPCC for **25 marks**.
- The student has to secure 40% of 25 marks to qualify in the CIE of the practical component of the IPCC

Experiment No: 1

CLIPPER & CLAMPER CIRCUITS

CLIPPER CIRCUITS

Aim: Conduct experiment to test diode clipping (single/double ended).

Apparatus Required:

S.No.	Particulars	Range	Quantity
1	Switching diode –	1N4007	1(One) No.
2	Resistors	10KΩ, 1K	1(One) No. Each
3	Bread board	1(One) No.	1(One) No.
4	Signal generator	1(One) No.	1(One) No.
5	Dual DC Regulated Power supply	(0 – 30) V	1(One) No.
6	CRO	--	1(One) No.
7	Connecting wires (Single Strand)	--	Few.
8	Multimeter	--	1(One) No.

Theory: Clippers are networks that employ diodes to clip away portions of an input signal without distorting the remaining part of the applied waveform. These clipper circuits transfer a selected portion of the input waveform to the output Diode clipping circuits are used to prevent a wave form from exceeding some particular limit either negative or positive or both. This is achieved by connecting the diode in serial or in parallel circuit. Variable DC voltage is connected in the circuit to achieve required level of clipping. By using different level DC voltages, it is possible to get different level of clipping in positive and negative side. These clipper circuits are also called as limiters.

Following are few types of clipper circuits

1. Single ended (positive or negative) and double ended clipping
2. Series or parallel based on the construction.

Peak detection is possible by connecting a suitable capacitor across the output of single ended clipping circuit. The capacitor charging time to be fast and discharging time to be slow so that capacitor holds the maximum value.

DESIGN:

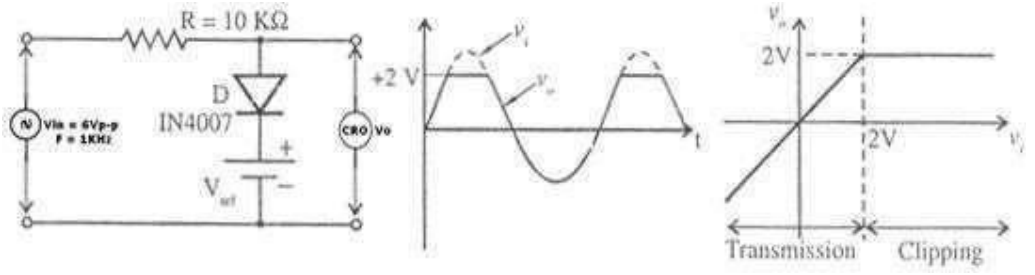
Assume Forward Resistance of Diode, R_f =100 Ω;Reverse Resistance of Diode, Rr =1MΩ

The series resistance is calculated such that $R = \sqrt{R_f . R_r} = \sqrt{100 \times 10^6} = 10K\Omega$

Note: If you are using 1N4001 R_f and R_r may be assumed to be 30 Ω and 300K Ω respectively and R=3.3 K Ω

The series resistor is used to limit the current through the diode.

Figure 1: Positive shunt clipper



If the output to be clipped above **2 V**, $\mathbf{V_{o\,(max)} = +2\ V}$

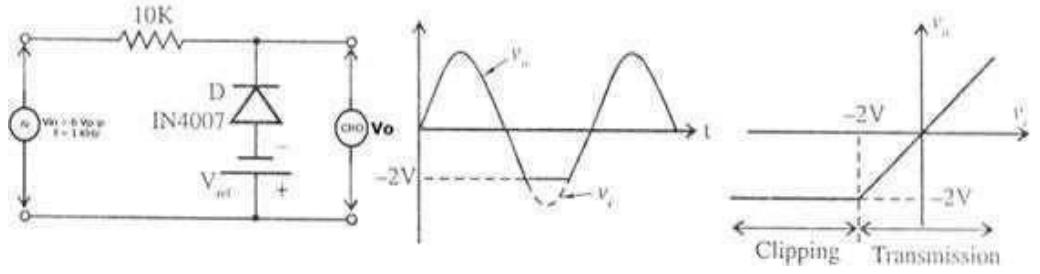
From the Fig.1 observe that when the diode is ON $V_{o\,(max)} = V_\gamma + V_{ref}$ where V_γ is Diode Cut-in Voltage which is equal to 0.6 V for IN4007 (Silicon diode)

Hence $\mathbf{V_{ref} = V_{o\,(max)} - V_\gamma}$

$\mathbf{= 2 - 0.6 = 1.4\ V}$

Make sure that the amplitude of the input sinusoidal signal is more than ±2Volts.

Figure 2: Negative shunt clipper



If the output to be clipped below – **2 Volts**.

From the Fig.2 observe that when the diode is ON $V_{o\,(min)} = -V_\gamma - V_{ref} = -2\ V = -0.6 - V_{ref}$;

$\therefore \mathbf{V_{ref} = 2 - 0.6 = 1.4\ V}$ $\mathbf{V_{ref} = 1.4\ V}$

Make sure that the amplitude of the input sinusoidal signal is more than ±2Volts.

Figure 3 : Positive series clipper

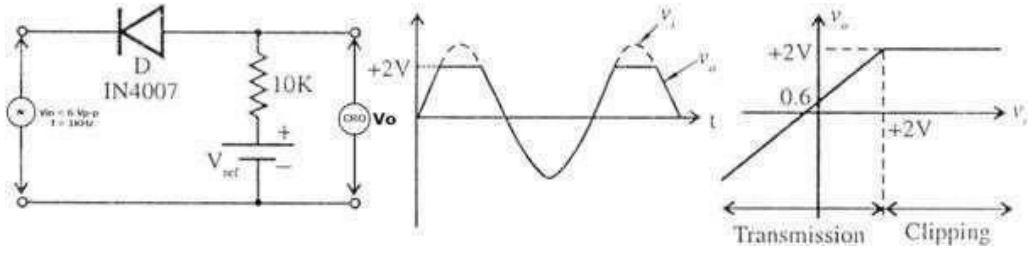


Figure 4: Negative series clipper

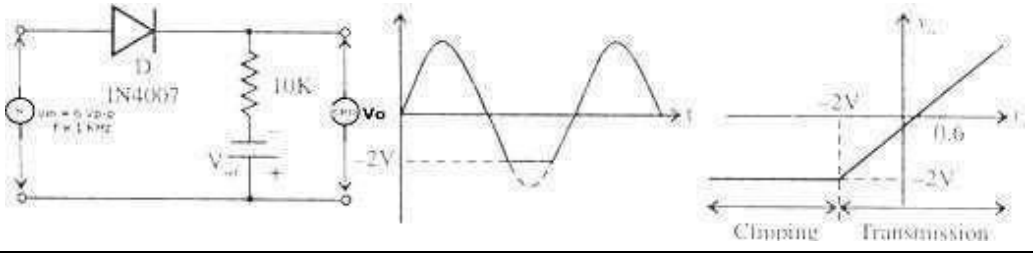
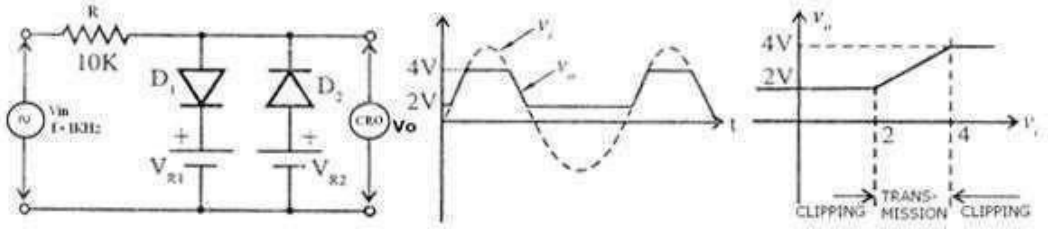


Figure 5: Double ended clipper with independent voltage levels



If the clipping the signal is required below 2 Volt and above 4 Volt then the design is as follows.

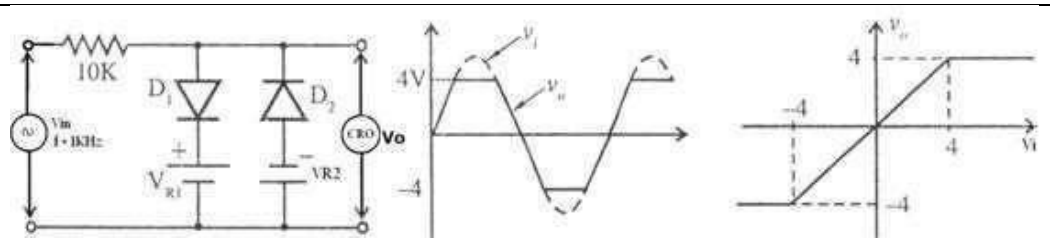
1. $Vo_{max} = 4$ V,

   $V_{o\,max} = V_{R1} + V_\gamma$; $V_{R1} = V_{o\,max} - V_\gamma = 4 - 0.6$; **$V_{R1}$ = 3.4 V**

2. $V_{o\,min} = 2$ V

   $V_{o\,min} = V_{R2} - V_\gamma$; $V_{R2} = V_{o\,min} + V_\gamma = 2 + 0.6$; **$V_{R2}$ = 2.6 V**

Figure 6: Double ended clipper with symmetrical voltage levels



If we need to generate a symmetrical clipping circuit with clipping voltage $V_0 = \pm 4$ Volts,

$V_{o\,max} = V_{R1} + V_\gamma = 4$ V; **V_{R1} = 4 – 0.6 = 3.4 V**

$V_{o\,min} = -V\gamma - V_{R2} = -4$ V**,** **V_{R2} = 4 – 0.6 = 3.4 V**

CLAMPER CIRCUITS

Aim: Conduct experiment to test diode clamping circuits (positive/negative).

Apparatus Required:

S.No.	Particulars	Range	Quantity
1	Switching diode –	1N4007	1(One) No.
2	Resistors	100KΩ, 1K	1(One) No. Each
3	Bread board	1(One) No.	1(One) No.
4	Signal generator	1(One) No.	1(One) No.
5	Dual DC Regulated Power supply	(0 – 30) V	1(One) No.
6	Capacitor	1uF/10uF	1(One) No.
7	CRO	--	1(One) No.
8	Connecting wires (Single Strand)	--	Few.
9	Multimeter	--	1(One) No.

Theory: Clamper is a circuit that "clamps" a signal to a different dc level without changing the appearance of the applied signal The different types of clampers are positive negative and biased clampers A clamping network must have a capacitor, a diode and a resistive element. The magnitude R and C must be chosen such that the time constant RC is large enough to ensure that the voltage across the capacitor does not discharge significantly during the interval the diode is non- conducting. By connecting suitable DC voltage in series with the diode, the level of swing can be varied.

Circuit Diagram

Positive peak clamper

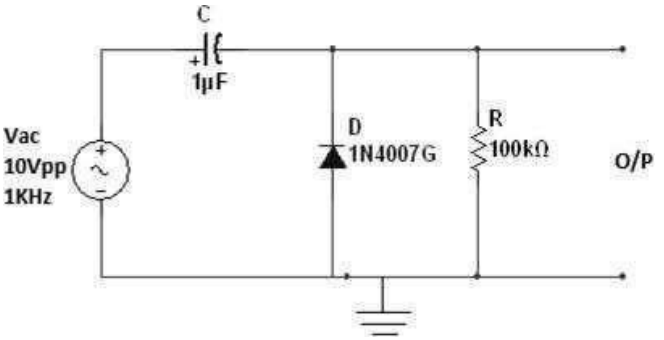


Figure 1: Positive clamper.

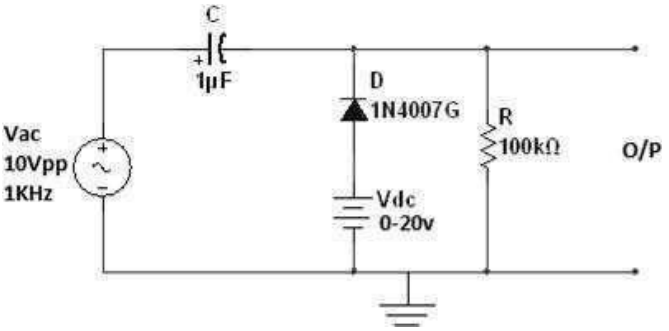


Figure 2: Positive clamper negative peak clamped.

Design: $V_{o,max} = V_{dc} + V_\gamma$; $V_\gamma = 0.6V$ (Silicon diode), $V_{dc} = V_{o,max} - V_\gamma$

To clamp the positive peak of a sine wave of 10 V (P – P) at +3V, we needVdc

= 3 – 0.6 = 2.4 V

Note: Changing this voltage changes the clamping level.

Let f = 1KHz. ∴ T = 1msec. Let **R = 10KΩ** (design procedure is same as that ofclipper)

For the circuit to perform satisfactorily RC = 10T

Therefore C = 10T / R = 10 x 1ms / 10KΩ; **C = 1.0 µF**

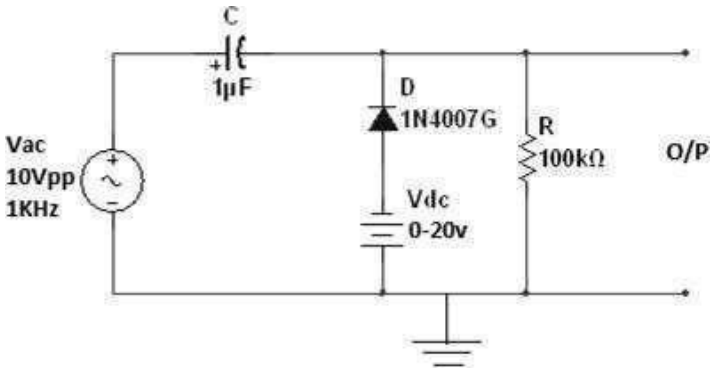


Figure 3: Positive clamper to clamp negative peak

$V_{o,max} = V_{dc} - V_{\gamma}$; Assume we need to clamp the negative peak to -3V, ie., $V_{o,max}$= **– 3V**
$V_{dc} = V_{o,max} + V_{\gamma}$,
V_{dc} = – 3 + 0.6 = – 2.4V (*Note: Changing this voltage changes the clamping level.)The design of R and C is as mentioned in earlier circuit*

Procedure:-

1. Set up the circuit on the bread board.
2. Switch on the signal generator and set voltage 10V P-P and frequency 1 KHz.
3. Using CRO measure the output wave form and sees that it matches with requiredwave form.
4. Repeat this for other clipper and clamper circuits.

Result: - All types of clipper and clamper circuits are tested and output wave form matches with the expected waveform.

Experiment No: 3

Static Transistor characteristics for CE, CB and CC modes and determination of h parameters.

Aim: To study the input and output characteristics of a transistor in Common Emitter configuration.

Apparatus Required:

S.No.	Particulars	Range	Quantity
1	Transistor	BC 107	1(One) No.
2	Resistors	1KΩ, 100KΩ	1(One) No. Each
3	Bread board	--	1(One) No.
4	Dual DC Regulated Power supply	(0 - 30 V)	1(One) No.
5	Digital Ammeters	(0 - 200 mA, 0-200	1(One) No. Each
6	Digital Voltmeter	(0 - 20V)	2(Two) No.
7	Connecting wires (Single Strand)	--	Few.

Theory:

- **TransistorCB(CommonBase)configuration**

It is transistor circuit in which base is kept common to the input and output circuits.

Characteristics:

• It has low input impedance (on the order of 50 to 500 Ohms).

• It has high output impedance (on the order of 1 to 10 Mega Ohms).

• Current gain (alpha) is less than unity.

- **TransistorCE(CommonEmitter)configuration**

It is transistor circuit in which emitter is kept common to both input and output circuits.

Characteristics (applications):

• It has high input impedance (on the order of 500 to 5000 Ohms).

• It has low output impedance (on the order of 50 to 500 Kilo Ohms).

• Current gain (Beta) is 98.

• Power gain is upto 37dB.

• Output is 180 degree out of phase.

- **TransistorCC(CommonCollector)configuration**

It is transistor circuit in which collector is kept common to both input and output circuits. It is also called as emitter follower.

Characteristics:

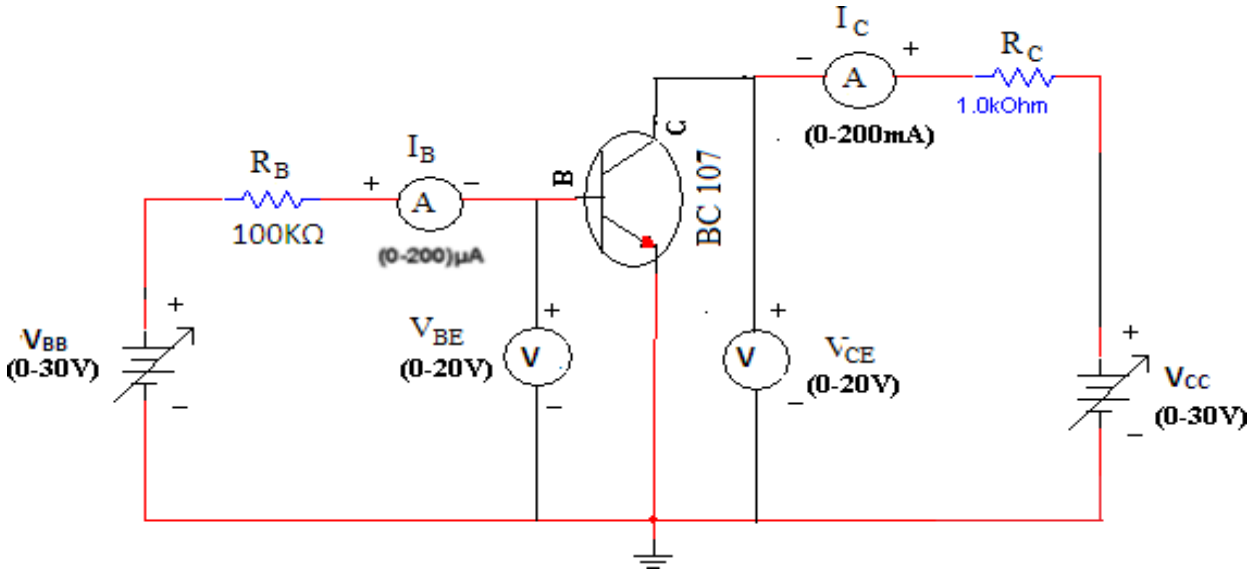
• It has high input impedance (on the order of about 150 to 600 Kilo Ohms).

• It has low output impedance (on the order of about 100 to 1000 Ohms).

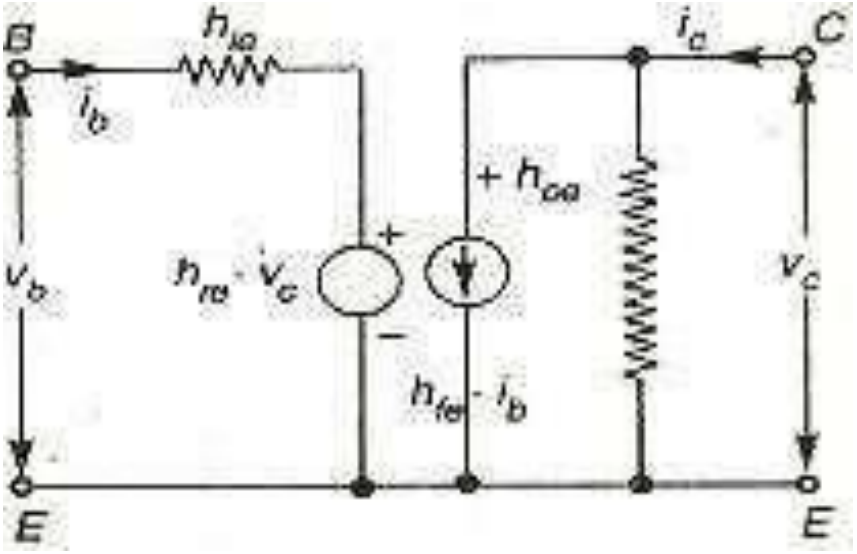
• Current gain (Beta) is about 99.

• Voltage and power gain is equal to or less than one.

Circuit Diagram:



h – Parameter model of CE transistor:

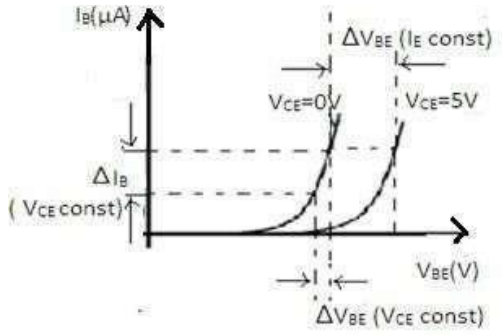


Observations:

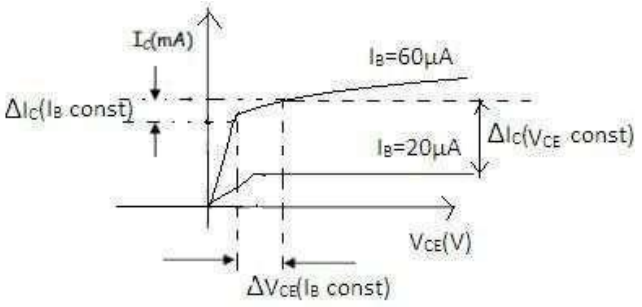
Input Characteristics				
V_{BB} (Volts)	V_{CE} = 0V		V_{CE} = 5V	
	V_{BE} (Volts)	I_B (µA)	V_{BE} (Volts)	I_B (µA)

Output Characteristics						
V_{CC} (Volts)	I_B = 0 µA		I_B = 20 µA		I_B = 40 µA	
	V_{CE} (Volts)	I_C (mA)	V_{CE} (Volts)	I_C (mA)	V_{CE} (Volts)	I_C (mA)

Graph:



Input Characteristics



Output Characteristics

Procedure:

Input Characteristics:

1. Connect the circuit as shown in the circuit diagram.
2. Keep output voltage V_{CE} = 0V by varying V_{CC}.
3. Varying V_{BB} gradually, note down base current I_B and base-emitter voltage V_{BE}.
4. Step size is not fixed because of non linear curve. Initially vary V_{BB} in steps of 0.1V. Once the current starts increasing vary V_{BB} in steps of 1V up to 12V.
5. Repeat above procedure (step 3) for V_{CE} = 5V.

Output Characteristics:

1. Connect the circuit as shown in the circuit diagram.
2. Keep emitter current I_B = 20 A by varying V_{BB}.
3. Varying V_{CC} gradually in steps of 1V up to 12V and note down collector current I_C and Collector-Emitter Voltage (V_{CE}).
4. Repeat above procedure (step 3) for I_B = 60µA, 0µA.

To Plot Graph:

1. Plot the input characteristics by taking V_{BE} on X-axis and I_B on Y-axis at a constant V_{CE} as a constant parameter.
2. Plot the output characteristics by taking V_{CE} on X-axis and taking I_C on Y-axis taking I_B as a constant parameter.

Calculations from Graph:

1. Input Characteristics: To obtain input resistance find ΔV_{BE} and ΔI_B for a constant V_{CE} on one of the input characteristics.
   Input impedance = $h_{ie} = R_i = \Delta V_{BE} / \Delta I_B$ (V_{CE} is constant) Reverse voltage gain = $h_{re} = \Delta V_{EB} / \Delta V_{CE}$ (I_B = constant)
2. Output Characteristics: To obtain output resistance find ΔI_C and ΔV_{CB} at a constant I_B.
   Output admittance 1/hoe = $R_o = \Delta I_C / \Delta V_{CE}$ (I_B is constant)
   Forward current gain = hfe = $\Delta I_C / \Delta I_B$ (V_{CE} = constant)

Result:

The h-parameters for a transistor in CE configuration are:

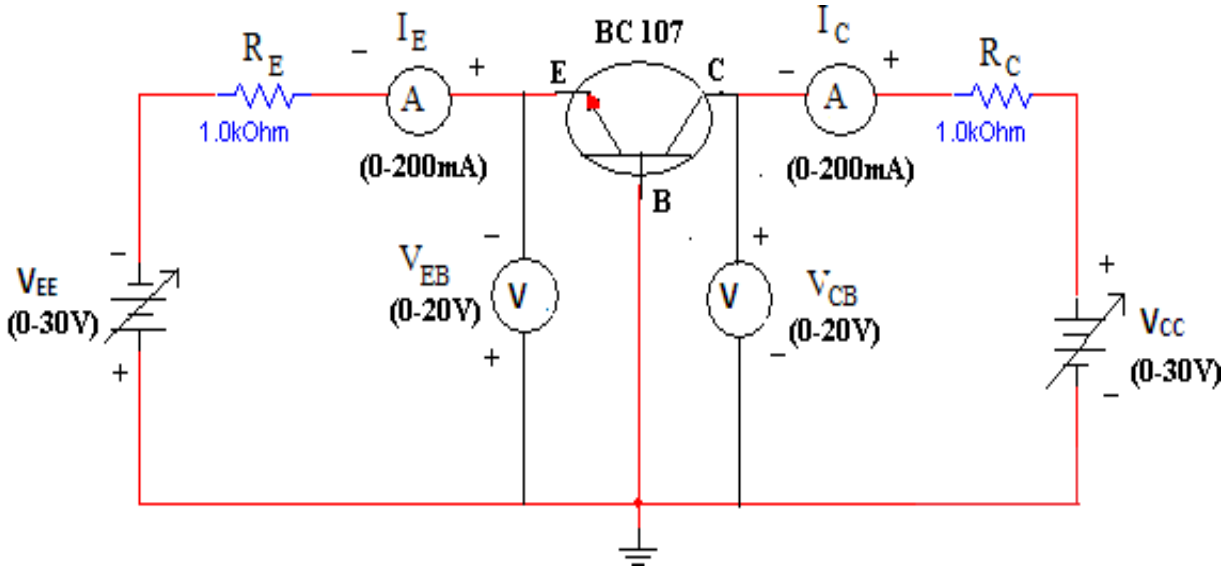
a. The Input Resistance (h_{ie}) _____Ohms.
b. The Reverse Voltage Gain (h_{re}) _____
c. The Output Conductance (h_{oe}) _____Mhos.
d. The Forward Current Gain (h_{fe}) _____.

Aim: To study the input and output characteristics of a transistor in Common Base Configuration.

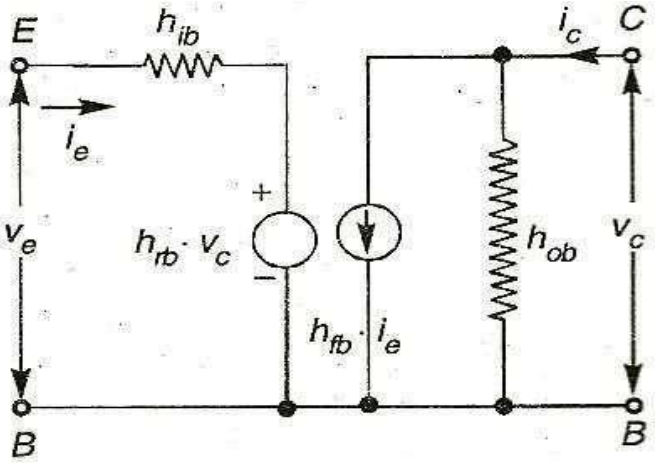
Apparatus Required:

S.No.	Particulars	Range	Quantity
1	Transistor	BC 107	1(One) No.
2	Resistors	1K	2(Two) No.
3	Bread board	--	1(One) No.
4	Dual DC Regulated Power supply	(0 - 30 V)	1(One) No.
5	Digital Ammeters	(0 - 200 mA, 0-200	1(One) No. Each
6	Digital Voltmeter	(0 - 20V)	2(Two) No.
7	Connecting wires (Single Strand)	--	Few.

Circuit Diagram:



h – Parameter model of CB transistor:

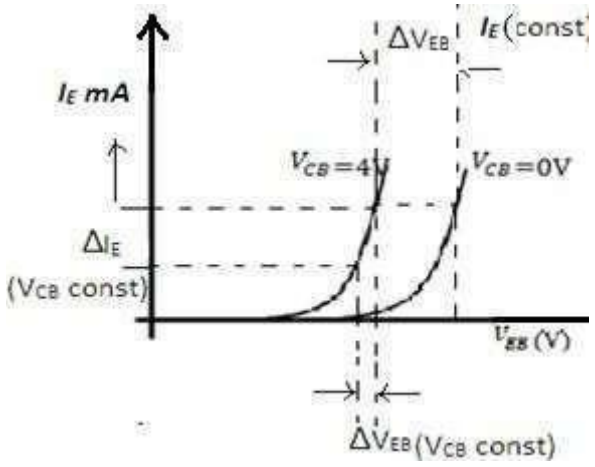


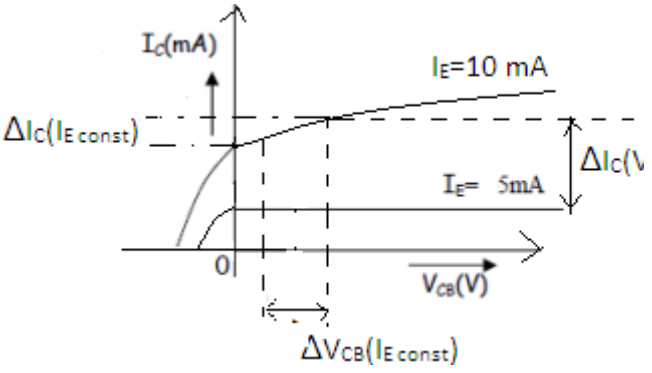
Observations:

Input Characteristics				
V_{EE} (Volts)	V_{CB} = 0V		V_{CB} = 4V	
	V_{EB} (Volts)	I_E (mA)	V_{EB} (Volts)	I_E (mA)

Output Characteristics						
V_{CC} (Volts)	I_E = 0mA		I_E = 5V		IE = 10mA	
	V_{CB} (Volts)	I_C (mA)	V_{CB} (Volts)	I_C (mA)	V_{CB} (Volts)	I_C (mA)

Graph:





1. Plot the input characteristics for different values of V_{CB} by taking V_{EE} on X-axis and I_E on Y-axis taking V_{CB} as constant parameter.
2. Plot the output characteristics by taking V_{CB} on X-axis and taking I_C on Y-axis taking I_E as a constant parameter.

Procedure:

Input Characteristics:

1. Connect the circuit as shown in the circuit diagram.
2. Keep output voltage V_{CB} = 0V by varying V_{CC}.
3. Varying V_{EE} gradually, note down emitter current I_E and emitter-base voltage(V_{EE}).
4. Step size is not fixed because of nonlinear curve. Initially vary V_{EE} in steps of 0.1 V. Once the current starts increasing vary V_{EE} in steps of 1V up to 12V.
5. Repeat above procedure (step 3) for V_{CB} = 4V.

Output Characteristics:

1. Connect the circuit as shown in the circuit diagram.
2. Keep emitter current I_E = 5mA by varying V_{EE}.
3. Varying V_{CC} gradually in steps of 1V up to 12V and note down collector current I_C and collector-base voltage (V_{CB}).
4. Repeat above procedure (step 3) for I_E = 10mA. 5.
   Repeat above procedure (step 3) for I_E = 10mA.

Calculations from Graph:

The h-parameters are to be calculated from the following formulae:

1. **Input Characteristics:** To obtain input resistance, find ΔV_{EE} and ΔI_E for a constant V_{CB} on one of the input characteristics.

   Input impedance = $h_{ib} = R_i =$ V_{EE} / I_E (V_{CB} = constant)
   Reverse voltage gain = hrb = $\Delta V_{EB} / \Delta V_{CB}$ (I_E = constant)

2. **Output Characteristics:** To obtain output resistance, find ΔI_C and ΔV_{CB} at a constant I_E.

   Output admittance = $h_{ob} = 1/Ro = \Delta I_C / \Delta V_{CB}$ (I_E = constant)
   Forward current gain = $h_{fb} = \Delta I_C / \Delta I_E$ (V_{CB} = constant)

Result:

The h-parameters for a transistor in CB configuration are:

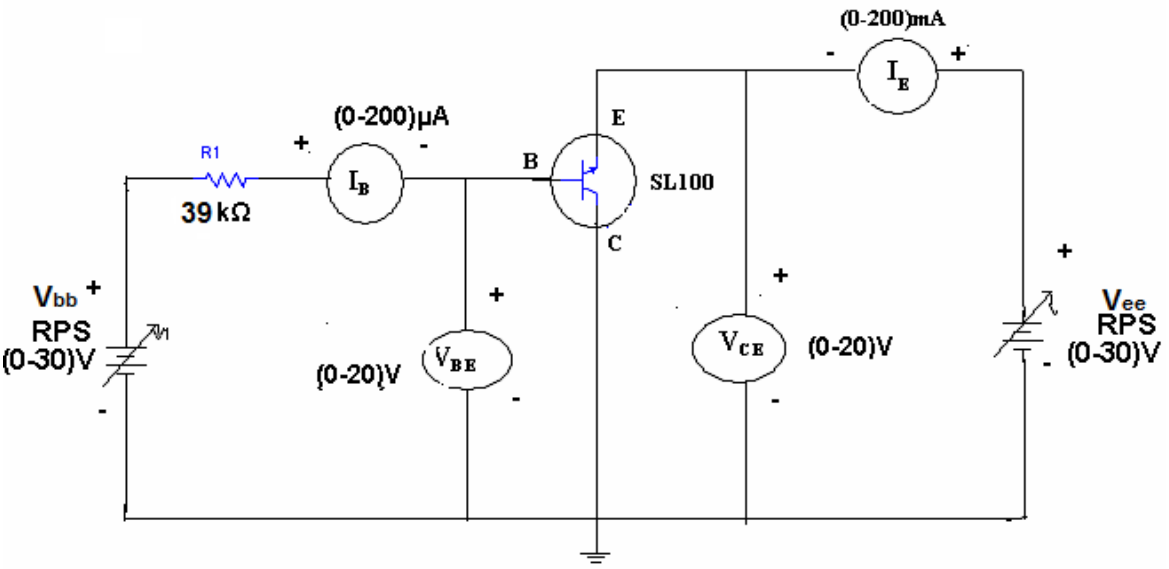
a. The Input resistance (h_{ib}) _____Ohms.
b. The Reverse Voltage Transfer Ratio (h_{rb})_____.
c. The Output Admittance (h_{ob}) _____Mhos.
d. The Forward Current gain (h_{fb}) _____.

Aim: To study the input and output characteristics of a transistor in Common Collector configuration.

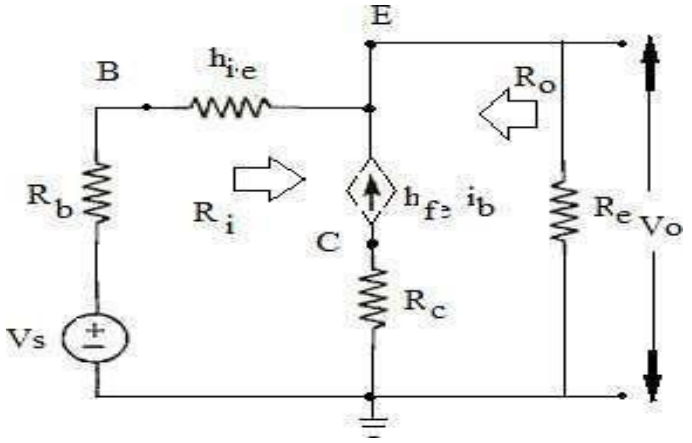
Apparatus Required:

S.No.	Particulars	Range	Quantity
1	Transistor	BC 107	1(One) No.
2	Resistors	39K , 1K	1(One) No. Each
3	Bread board	--	1(One) No.
4	Dual DC Regulated Power supply	(0 - 30 V)	1(One) No.
5	Digital Ammeters	(0 – 300µA, 0-10mA)	1(One) No. Each
6	Digital Voltmeter	(0-10V, 0-1V)	2(Two) No.
7	Connecting wires (Single Strand)	--	Few.

Circuit Diagram:



h – Parameter model of CB transistor:

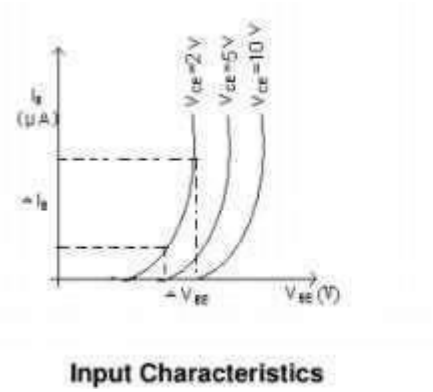


Observations:

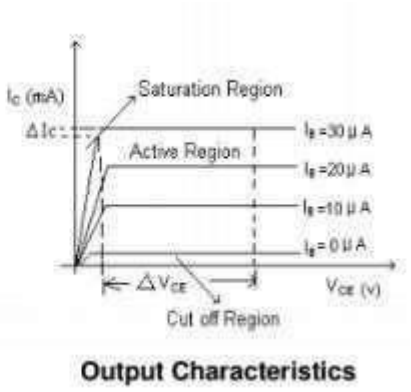
Input Characteristics							
Sl. No	Applied Voltage V_{BB} (V)	V_{CE} = 2V		V_{CE} = 5V		V_{CE} = 10V	
		V_{BE} (V)	I_B (µA)	V_{BE} (V)	I_B (µA)	V_{BE} (V)	I_B (µA)
1							
2							
3							
4							
5							

Output Characteristics							
Sl. No	Applied Voltage V_{CC} (V)	I_B = 10µA		I_B = 20µA		I_B = 30µA	
		V_{CE} (V)	I_E (mA)	V_{CE} (V)	I_E (mA)	V_{CE} (V)	I_E (mA)
1							
2							
3							
4							
5							

Graph:



Input Characteristics



Output Characteristics

1. Plot the input characteristics for different values of $\mathbf{V_{CE}}$ by taking $\mathbf{V_{BE}}$ on X-axis and $\mathbf{I_B}$ on Y-axis taking $\mathbf{V_{CC}}$ as constant parameter.
2. Plot the output characteristics by taking $\mathbf{V_{CE}}$ on X-axis and taking $\mathbf{I_C}$ on Y-axis taking $\mathbf{I_B}$ as a constant parameter.

Procedure:

Input Characteristics:

1. Connect the circuit as shown in the circuit diagram.
2. Keep output voltage V_{CE} as constant 2V by varying V_{CC}.
3. Varying V_{BB} gradually, note down base current I_B and emitter-base voltage (V_{BE}).
4. Step size is not fixed because of nonlinear curve. Initially vary V_{EE} in steps of 0.1 V. Once the current starts increasing vary V_{BB} in steps of 1V up to 12V.
5. Repeat above procedure (step 3) for V_{CE} = 5V & 10V.

Output Characteristics:

1. Fix base current, I_B at constant value say 10µA.
2. Vary the output voltage V_{CC} in steps.
3. Measure the voltage V_{CE} and current I_C for different values.
4. Repeat above steps for I_B = 20µA, 30µA
5. Draw output static characteristics for tabulated values.

Calculations from Graph:

The h-parameters are to be calculated from the following formulae:

1. **Input Characteristics:** To obtain input resistance, find ΔV_{EE} and ΔI_E for a constant V_{CB} on one of the input characteristics.

   Input impedance = $h_{ic} = R_i = \Delta V_{BB} / \Delta I_B$ (V_{CE} = constant) Reverse voltage gain = $h_{rb} = \Delta V_{CE} / \Delta V_{BC}$ (I_B = constant)

2. **Output Characteristics:** To obtain output resistance, find ΔI_E and ΔV_{CE} at a constant I_B.

   Output admittance = $h_{oc} = 1/Ro = \Delta I_E / \Delta V_{CE}$ (I_B = constant) Forward current gain = $h_{fc} = \Delta I_E / \Delta I_B$ (V_{CE} = constant)

Result:

The h-parameters for a transistor in CC configuration are:

a. The Input resistance (h_{ic}) _____ Ohms.

b. The Reverse Voltage Transfer Ratio (h_{rc}) _____.

c. The Output Admittance (h_{oc}) _____ Mhos.

d. The Forward Current gain (h_{fc}) _____.

Experiment No: 4

RC – COUPLED SINGLE STAGE BJT AMPLIFIER

Aim: To find the Frequency response of single stage BJT and FET RC coupled amplifier and determination of half power points, bandwidth, input and output impedances.

Apparatus Required:

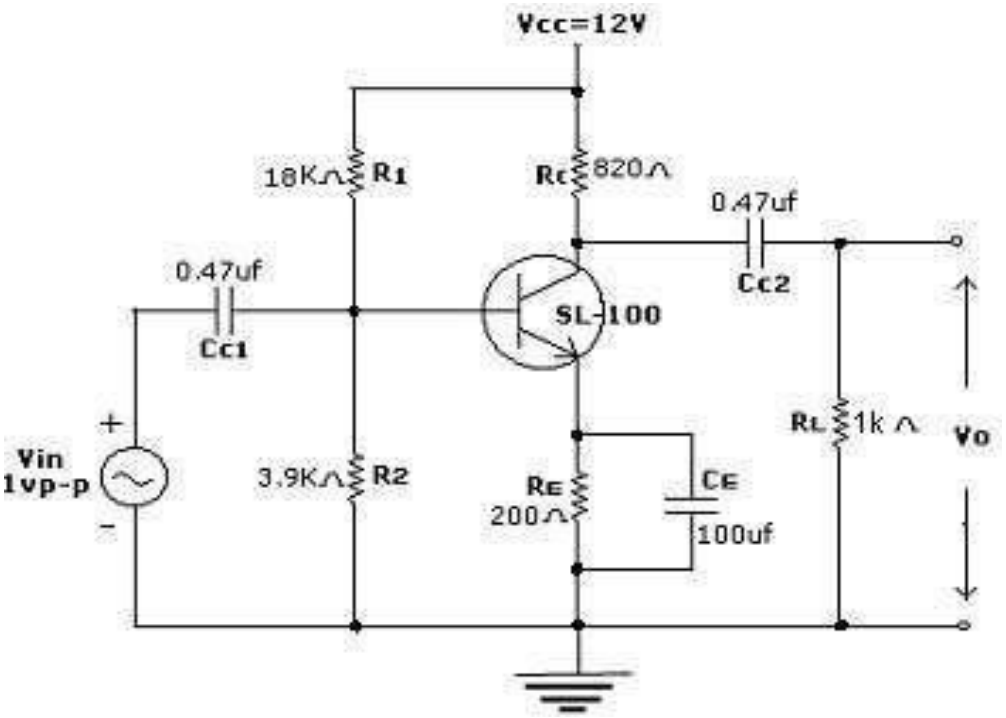
S.No	Particulars	Range	Quantity
1.	Transistor	SL100	01
2.	Capacitors	0.47μF 100μF	02 01
3.	Resistors	18kΩ 3.9kΩ 820kΩ, 220kΩ, 10kΩ	01 01 01 01 01
4.	Regulated Power Supply	0-32 V	01
5.	Signal Generator	---	01
6.	Oscilloscope and Probes	---	01
7.	Bread Board	---	01
8.	Connecting wires	---	Few

Theory:

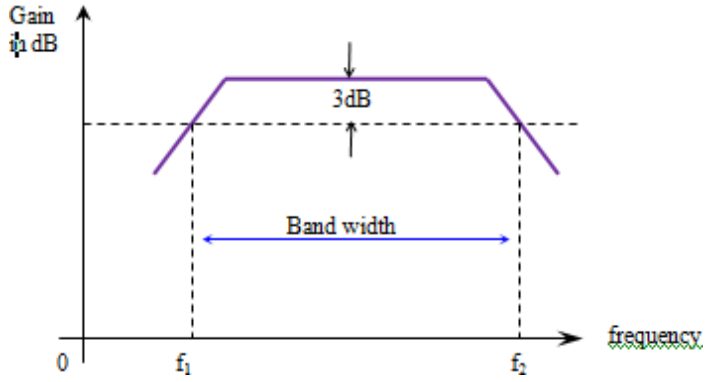
The R-C coupled amplifier is widely used as an audio amplifier because of it's good frequency response, low cost and simplicity. It is a transistor amplifier in the **C-E configuration.** The C-E configuration is preferred because of its large voltage and current gains, medium input impedance and medium output impedance. It consists of a collector resistance $\mathbf{R_C}$ which is mainly responsible for developing the output voltage. An emitter resistance $\mathbf{R_E}$ which is used to provide operating point stability. Resistor $\mathbf{R_{B1}}$ is a voltage divider bias resistor which provides the required reverse bias voltage across collector base junction. $\mathbf{R_{B2}}$ is the second biasing resistor of the network which provides the required forward bias voltage across base-emitter junction. Capacitor $\mathbf{C_{in}}$ is used to couple the ASG to the amplifier ie. to isolate the ASG from the biasing network with respect to DC conditions. $\mathbf{C_{out}}$ is a capacitor used to isolate the amplifier circuit from the load with respect to DC. The bypass capacitor $\mathbf{C_E}$ is used to provide a bypass path for AC signals and there by reduces the current feedback which will reduce the amplifier gain considerably. The input signal is applied between base and emitter so that it drives an AC base current. Due to transistor action, this input current results in a collector current $\mathbf{I_C = \beta I_B}$, where β is the current gain of transistor in common emitter configuration. The output voltage is therefore amplified but suffers a phase shift of 180.

The magnitude of the input signal should be such that the operating point always remain well within the active region, if not the output waveform would be clipped (i.e the transistor is driven into saturation or cut-off by positive and negative input peaks respectively).The coupling capacitor **C_{in}** and **C_{out}** are mainly responsible for limiting the value of lower cut-off frequency **(LCF→f1)** while the device junction capacitance is responsible for limiting the values of upper cut-off frequency **(UCF→f2).**

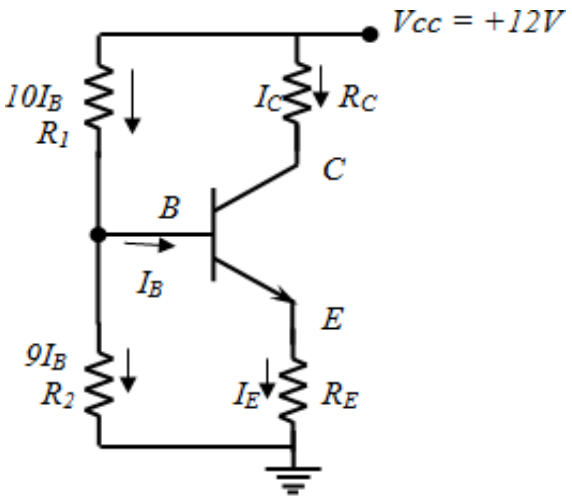
Circuit Diagram:



Frequency Response:



Design:



Biasing Circuit

Let V_{CC} =10V, I_C = 5 mA, β=100

To find R_E:

$V_{RE} = V_{CC}/10 = 10/10 = 1$ $I_E.R_E = 1V$

$R_E = 1\ V/\ I_E = 1V / Ic = 1V/5mA = 200\ \Omega$

R_E =200 Ω

For R_C, $V_{CE} = Vcc/2 = 10/2 = 5$ V

Applying KVL in C-E Loop $V_{CC} - I_C R_C - V_{CE} - V_{RE} = 0$

$10 - 5\times10^{-3}\times R_C - 5 - 1 = 0$

R_C= 800 Ω

To find R_1:

From the above biasing circuit

$V_B = V_{BE} + V_{RE} = 0.7 + 1 = 1.7$ V

$Ic = \beta.I_B$ or $I_B = Ic/\beta = 500mA/100 = 0.5$ mA

Assume that a current 10 I_B flows through R_2

$R_1 = (V_{CC} - V_B)/\ 10I_B = (10-1.7)/\ 10\times\ 0.5 = 16.6\ \Omega$

Choose R_1 as 18kΩ

Assuming 9IB flows through R_2

$R_2 = V_B / 9I_B = \{1.7/9\} \times 0.5 = 3.7\ k\Omega$

Choose R_2 as 3.9kΩ

Bypass capacitor C_E and coupling C_{C1} and C_{C4} Let $X_{CE} = R_E.1/10$ at f = 100Hz

i.e, $1/2\pi f_C = R_E/10$

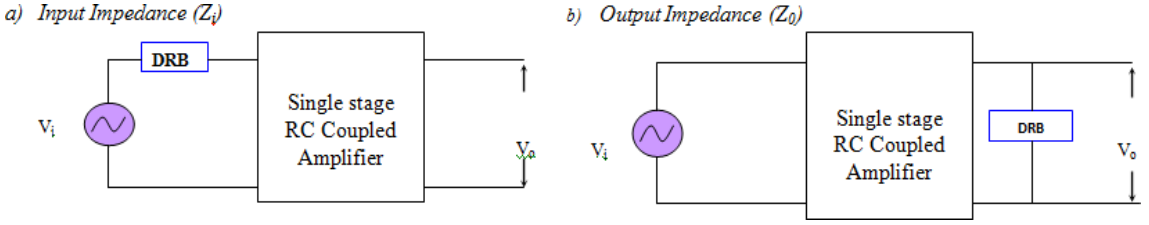
$C_E = 10 / (2\pi \times 100 \times 220) = 72.3\ \mu F$

Choose C_E = 100 μF $C_{C1} = C_{C2}$ = 0.47 μF

Procedure:

1. Connect the biasing circuit as shown in the figure -2, set the RPS voltage Vcc = 12V. Measure the DC voltages (Using Oscilloscope) V_B at the base, V_C at the collector and V_E at the emitter with respect to ground. Then determine
   $V_{CE} = V_C - V_E =$ _____ V
   $I_C =$ $\frac{V_{cc}-V_c}{R_c}$ = _____ mA (then Q point is given by V_{CE}, I_C)
2. Connect the RC coupled amplifier circuit shown in figure-1.
3. Apply the input sine wave at frequency say 10KHz from the signal generator and adjust peak–to-peak amplitude (Vi) of **20 to 50 milli volts** (till maximum undistorted sine wave output is obtained).
4. Vary the input sine wave frequency from 10Hz to 1MHz in suitable steps and measure the output voltage V_0 of the amplifier at each step using Oscilloscope(Keeping input amplitude remains constant throughout the frequency range) and record the readings in the tabular column.
5. Calculate the Gain in dB
6. Plot the graph of gain in dB v/s the frequency in semi log graph sheet and determine lower cutoff frequency (f_1), upper cutoff frequency (f_2), mid band voltage gain A_{mid}, and gain bandwidth product (GBW).

Determination of Input Impedance (Z_i) and Output Impedance (Z_0)



Procedure: For measuring the input impedance "Z_i"

1. Connect the circuit as shown in fig.3
2. Set the following.
   i) DRB to its minimum value "0"
   ii) Input sine wave amplitude is kept at 50mV.
   iii) Frequency around 10 kHz.
   iv) Measure p-p V_o
3. Let $V_o = V_a$, Increase DRB till $V_o = V_a/2$. So that the corresponding DRB value gives the input impedance "Z_i" of the RC Coupled amplifier.

Procedure: For measuring the output impedance "Z_O"

1. Connect the circuit as shown in fig.4
2. Set the following.
   i. DRB to its Maximum value.
   ii. Input sine wave amplitude is kept at 50mV
   iii. Frequency around 10 kHz.

iv. Measure p-p V_o

Let $V_o = V_b$, Decrease DRB till $V_o = V_b/2$

3. So that the corresponding DRB value gives the Output impedance "Z_o" of the RC Coupled amplifier

Observations:

V_{in} = 50 $mV_{(p-p)}$

Sl.No	Freq in Hz	V_o in Volts	$A_v=V_o/V_{in}$	Gain in dB $20\log V_o/V_{in}$
1	200Hz			
2	400Hz			
3	600Hz			
4	800Hz			
5	1k			
6	2k			
7	3K			
8	4K			
9	5K			
10	6K			
11	7K			
12	8K			
13	9K			
14	10K			
15	30K			
16	50K			
17	70K			
18	100K			
19	300K			
20	500K			
21	700K			
22	1MHz			
23	1.5MHz			
24	2MHz			

Results:

- Mid band voltage gain = _____
- Mid band voltage gain in dB = _____ dB
- Lower cutoff frequency = _____HZ
- Upper cutoff frequency = _____Hz
- Band width = _____Hz
- Gain Bandwidth Product = _____ Hz
- Input Impedance = _____Ω
- Output Impedance = _____Ω

Experiment No: 5

BJT RC PHASE SHIFT OSCILLATOR

Aim: To design and test the performance of RC Phase shift Oscillator for the given frequency of oscillation.

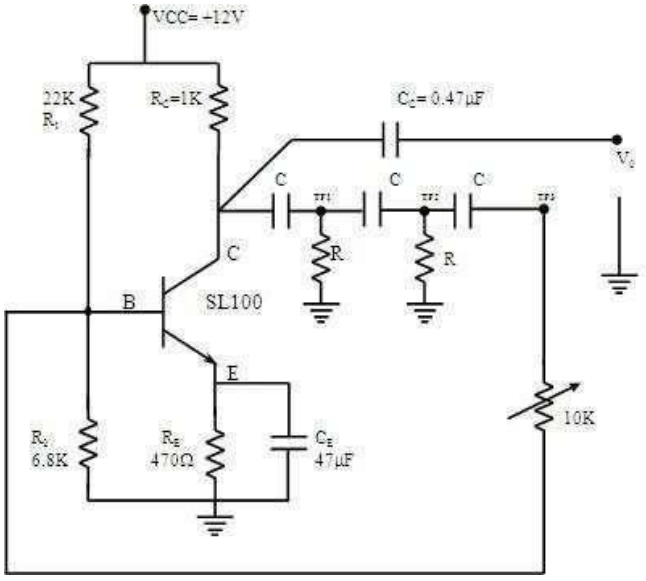
Apparatus required:

S.No.	Particulars	Range	Quantity
1.	Transistor	SL100	01
2.	Capacitors	0.1μF 0.01μF 47μF	01 03 01
3.	Resistors	22 KΩ 6.8 KΩ 1 KΩ 2.2 KΩ 470 Ω	01 01 01 02 01
4.	Regulated Power Supply	0-30V	01
5.	Potentiometer	10 KΩ	01
6.	Oscilloscope and Probes	---	01
7	Bread Board	--	01
8	Connecting wires	---	few

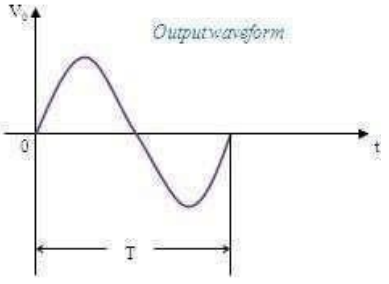
Theory:

The R-C phase shift oscillator is widely used to generate audio frequency oscillations. Figure shows the circuit diagram of a R-C phase shift oscillator. It consists of a conventional R-C phase shifting network (phase lead). The phase shift network consists of three sections R_1C_1, R_2C_2 and R_3C_3. At some particular frequency the phase shift in each R-C sections 60° ie, the total phase shift produced by the three stages R-C network is 180°. The frequency of oscillation is given by: $F_{th} = 1/(2\pi RC\sqrt{6})$, where, $R_1 = R_2 = R$ and $C_1 = C_2 = C$

Circuit diagram:



SPECIMEN GRAPH:



Design:

Amplifier design:

Let V_{CC} *= 12V,* I_C *= 4mA,* h_{fe} *= 100 (for SL100) Let* V_E *= 2V,* V_{CE} *= 6V*

Therefore, $R_E = V_E/I_E = V_E/I_C = 2/4\text{mA} = 0.5\ K\Omega = 500\Omega$

Use $\boldsymbol{R_E = 470\Omega}$

R_C*: From the biasing circuit (apply KVL to CE loop)* $V_{CC} - I_C R_C - V_{CE} - V_E = 0$

$12 - 4R_C - 6 - 2 = 0$

Therefore $\boldsymbol{R_C = 1\ K\Omega}$

Calculation of R_1 AND R_2

From the biasing circuit

$$V_B = V_{CC} X \frac{R_2}{R_1 + R_2}$$

We know that $V_B = V_{BE} + V_E$

$V_B = 2 + 0.7 = 2.7V$

Therefore

$$V_B = \frac{R2}{R1 + R2} V_{CC}$$

$$\frac{2.7}{12} = \frac{R2}{R1 + R2}$$

$$0.225 = \frac{R2}{R1 + R2}$$

$0.225R_1 + 0.225R_2 = R_2$

$R_1 = 3.44R_2$

If $\boldsymbol{R_2 = 6.8\ K\Omega}$*, then* $R_1 = 23.3K\Omega$*, Use* $R_1 = 22K\Omega$

Use $\boldsymbol{C_E = 50\mu F \text{ or } 47\ \mu F}$ *(Electrolytic)*

Also use $\boldsymbol{C_C = 0.1\mu F}$ *(ceramic)*

Design of RC shifting network

The frequency of oscillations is determined by phase shifting network. The oscillating frequency for the above circuit is given by

$$f_0 = \frac{1}{2\pi RC\sqrt{6 + 4K}}$$

Where $K = \frac{R_C}{R}$ *which is usually < 1*

Let $\boldsymbol{f_0 = 2\ KHz}$ *(Audio frequency range 20Hz to 20KHz) and* $\boldsymbol{R = 2.2\ K\Omega}$

Therefore $K = \frac{R_C}{R} = \frac{1K}{K} = 0.454$

Therefore $fo = \frac{1}{2\pi RC\sqrt{6 + 4(0.454)}}$

$C = 0.0121\ \mu F$; ***Use C = 0.01*** μF

Note:

The last resistor in the phase shifting network is chosen to be a 10K pot. This is to get an overall phase shift of 180^o at frequency of oscillations.

The minimum h_{fe} required for the transistor to oscillate is

$$h_{fe(min)} = 23 + 29\ x\ \frac{R}{R_C} + 4\ x\ \frac{R^C}{R}$$

Where $R_C = 1K\Omega$ *and* $R = 2.2K\Omega$ *(Phase shifting network)*

Therefore $h_{fe(min)} = 23 + 29\ x\ \frac{2.2K}{1K} + 4\ x\ \frac{1K}{K}$

$h_{fe(min)} = 89$

Procedure:

1. Connections are made as per the circuit diagram.
2. Switch ON the power supply and set the biasing voltage V_{CC} =12V.
3. Adjust the 10KΩ pot to get a stable sinusoidal output and observe the sine wave form on oscilloscope.
4. Measure the frequency of oscillations of the output from the oscilloscope, then compare with theoretical value.
5. With respect to the output Vo, the waveforms at points TP_1, TP_2 and TP_3, are observed on oscilloscope. We can see the phase shift at each point being shifted by an angle 60^0, 120^0, 180^0.
6. Draw the waveform on graph sheet.

Result:

Theoretical frequency of oscillations =_____KHz

Practical frequency of oscillations =_____KHz

Experiment No: 7

STUDY OF COLPITTS OSCILLATOR.

AIM:

To design and set up a Colpitts oscillator using BJT and toobserve the sinusoidal output waveform.

APPARATUS REQUIRED:

S.NO	APPARATUS	SPECIFICATION	QUANTITY
1.	Transistor	BC 107	1
2.	Resistors	11.64 KΩ, 552.2Ω,10.02KΩ1.67kΩ	Each 1
3.	Capacitors	53.5nF,80µF, 100mF	2,1,1
4.	Inductor	0.78mH	1
5.	RPS	±12V	1
6.	CRO	1MHz	1
7.	Connecting wires	-	Req.

THEORY:

A Colpitts oscillator is the electrical dual of a Hartley oscillator, where the feedback signal is taken from an "inductive" voltage divider consisting of two coils in series (or a tapped coil). Fig. 1 shows the common-base Colpitts circuit. L and the series combination of C_1 and C_2 form the parallel resonant tank circuit which determines the frequency of the oscillator. The voltage across C_2 is applied to the base-emitter junction of the transistor, as feedback to create oscillations. Fig. 2 shows the common-collector version. Here the voltage across C_1 provides feedback. The frequency of oscillation is approximately the resonant frequency of the LC circuit, which is the series combination of the two capacitors in parallel with the inductor

$$f_0 = \frac{1}{2\pi\sqrt{L\left(\frac{C_1C_2}{C_1+C_2}\right)}}$$

DESIGN PROCEDURE:

Select a appropriate transistor and note down its specification such as V_{CE},$I_{C(MAX)}$, $h_{fe(min)}$ and $V_{be(sat)}$.

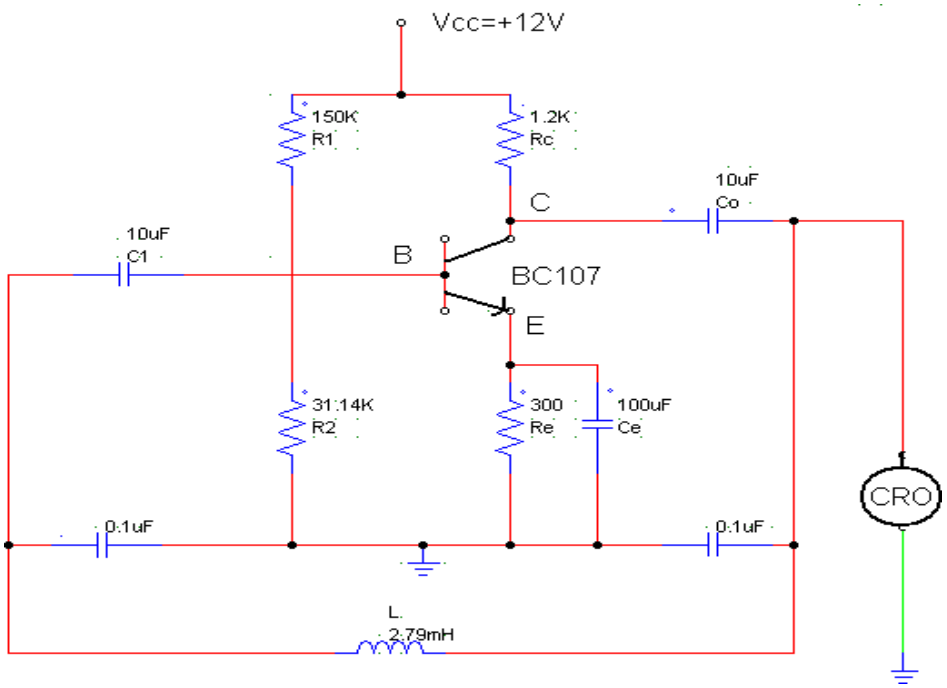
- $V_{CC}= V_{CEQ}$
- $R_2=S* R_E$
- $V_{CC}[R_2/(R_1+ R_2)= V_{BE}+V_{BE(SAT)}$
- $V_{R1}+V_{R2}=V_{CC}$

- $h_{fe} \geq C_1 * C_2/(C_1 + C_1)$
- $X_{CE} \leq R_E/10$

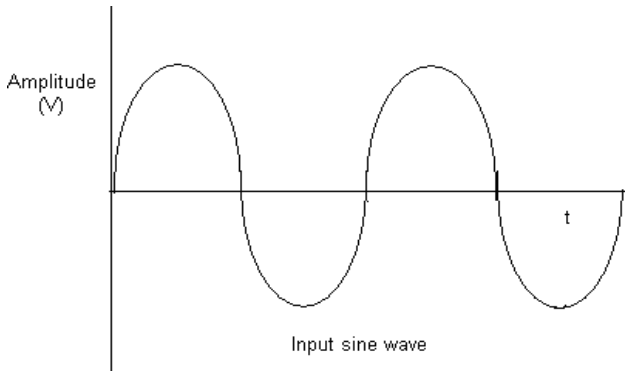
PROCEDURE:

- Hook up the circuit as shown in the circuit diagram.
- Switch on the power supply.
- Slight modification in value of C_1 and C_2 can be made to get perfect sine wave output.
- Observe the output waveform in CRO.

CIRCUIT DIAGRAM:



MODEL GRAPH:



TABULATION:

Amplitude(Volts)	Time(ms)	Frequency (KHz)

RESULT: Thus the Colpitts oscillator was designed and its output waveform was verified.

STUDY OF HARTLEY OSCILLATOR

To design and set up a Hartley oscillator using BJT and toobserve the sinusoidal output waveform.

APPARATUS REQUIRED:

S.NO	APPARATUS	SPECIFICATION	QUANTITY
1.	Transistor	BC 107	1
2.	Resistors	2.74 KΩ, 1.76KΩ,10.58KΩ	1,2,1
3.	Capacitors	0.1μF, 0.1μF	Each 2
4.	Inductor	0.1mH,0.33mH	Each 1
5.	RPS	±12V	1
6.	CRO	1MHz	1
7.	Connecting wires	-	Req.

THEORY:

The **Hartley oscillator** is an electronic oscillator circuit in which the oscillation frequency is determined by a tuned circuit consisting of capacitors and inductors, that is, an LC oscillator. The Hartley oscillator is distinguished by a tank circuit consisting of two series-connected coils (or, often, a tapped coil) in parallel with a capacitor, with an amplifier between the relatively high impedance across the entire LC tank and the relatively low voltage/high current point between the coils. The Hartley oscillator is the dual of the Colpitts oscillator which uses a voltage divider madeof two capacitors rather than two inductors. Although there is no requirement for there to be mutual coupling between the two coil segments, the circuit is usually implemented using a tapped coil, with the feedback taken from the tap, as shown here. The optimal tapping point (or ratio of coil inductances) depends on the amplifying device used, which may be a bipolar junction transistor.

DESIGN PROCEDURE:

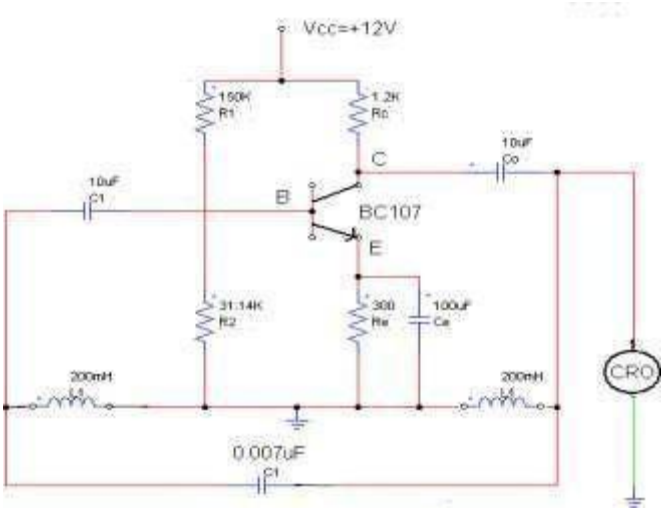
Select a appropriate transistor and note down its specification such as V_{CE},$I_{C(MAX)}$, $h_{fe(max)}$ and $V_{be(sat)}$.

- $V_{CC}= V_{CEQ}+ I_{CQ}(R_C+R_E)$
- $R_2=S* R_E$
- $V_{CC}[R_2/(R_1+ R_2)= V_{BE}+V_{BE(SAT)}$
- $V_{R1}+V_{R2}=V_{CC}$

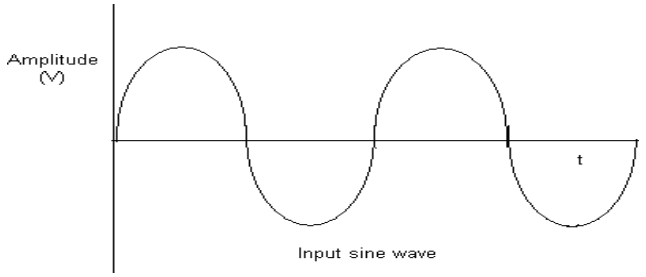
PROCEDURE:

- Hook up the circuit as shown in the circuit diagram.
- Switch on the power supply.
- Slight modification in value of L_1 and L_2 can be made to get perfect sinewave output.
- Observe the output waveform in CRO.

CIRCUIT DIAGRAM:



MODEL GRAPH:



TABULATION:

Amplitude(Volts)	Time(ms)	Frequency (KHz)

RESULT: Thus the Hartley oscillator was designed and its output waveform was verified.

Experiment No: 8

DARLINGTON EMMITTER FOLLOWER

Aim: To determination of gain, input and output impedance of BJT Darlington emitter follower with and without bootstrapping.

Apparatus Required:

S.N	Particulars	Range	Quantity
1.	Transistor	SL100	01
2.	Capacitors	0.1μF 0.01μF 47μF	01 03 01
3.	Resistors	22 KΩ 6.8 KΩ 1 KΩ 2.2 KΩ 470 Ω	01 01 01 02 01
4.	Regulated Power Supply	0-30V	01
5.	Signal Generator	---	01
6.	Voltmeter	---	01
7.	Ammeter	---	01
8.	CRO and Probes	---	01
9.	Bread Board	--	01
10.	Connecting wires	---	few

Theory:

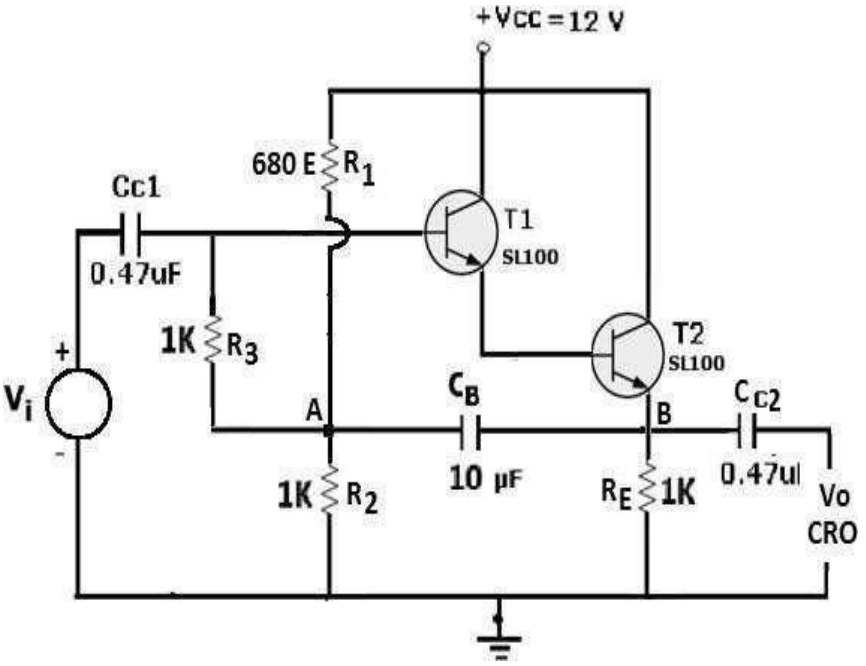
A Darlington pair behaves like a single transistor, meaning it has one base, collector, and emitter. It typically creates a high current gain (approximately the product of the gains of the two transistors, due to the fact that their β values multiply together). A general relation between the compound current gain and the individual gains is given by:

$$\beta_{\textbf{Darlington}} = \beta_1 . \beta_2 + \beta_1 + \beta_2$$

If β_1 and β_2 are high enough (hundreds), this relation can be approximated with:

$$\beta_{\text{Darlington}} \approx \beta_1 . \beta_2$$

Circuit Diagram:



Design:

Let V_{CC} = 12 V D.C.; $I_{C2} \approx I_{E2}$ = 6mA, $h_{fe}1$ = 50, $h_{fe}2$ = 100;

Choose VCE2 = VCC / 2 = 12/2 = 6V;

$I_{B2}=I_{C2}/h_{fe}2$ = 6000/100 = 60µA = I_{C1};

$I_{B1} = I_{C1}/h_{fe1}$= 60/50 = 1.2µA

$R_E = (V_{CC} – V_{CE2})/I_{E2}$ =6V / 6mA = 1000 Ω

Assume R_3 = 1K, then R_3I_{B1} = 1.2 mV.

$V_{AG} = V_{AB1} + V_{BE1} + V_{BE2} + V_{E2}$

$= R_3I_{B1} + V_{BE1} + V_{BE2} + V_{E2}$

=1.2 mV + 0.7 V + 0.7 V + 6V

=7.4012 V

With R_2 = 1 K, $I_{R2} = V_{AG}/R_2$ = 7.4012 mA=7401.2 µA, let R_2 = 1 K

Therefore, $I_{R1} = I_{R2} + I_{B1}$ =7401.2 + 1.2 = 7402.4 µA

$R_1= (V_{CC}-V_{AG})/I_{R1}$ = 12-7.4012/7402.4 µA =621.258Ω; let R1 = 680 Ω

Choose $C_{C1} = C_{C2}$ = 0.47 µF.

Procedure:

To measure Voltage Gain

1. Connect the circuit as shown in the figure
2. Switch on the power supply and set V_{CC} = +12 V.

3. Measure the DC Voltages using CRO or Multimeter and record.

	V_{CE1}	V_{BE1}	V_{CE2}	V_{BE2}	V_{E2}
Assumed	6V	0.7V	6V	0.7V	6V
Obtained					

4. Apply a sine wave voltage from the Function Generator.
5. Observe the o/p Vo. Measure and record Vi and Vo. Compute and enter the voltage gain, $A_V=V_O/V_i$ in the table.

Voltage gain with bootstrap

Vi							Vi, max
Vo							
Av							

Record V_i, Max, The maximum input you can apply for undistorted output as the Maximum Signal handling capacity" of the Emitter follower.

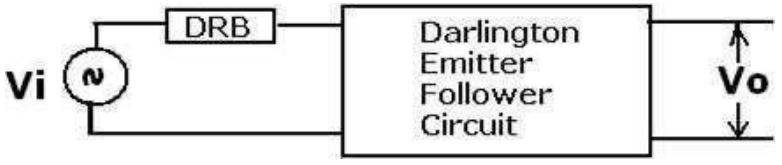
6. Repeat the experiment after disconnecting the capacitor CB in branch AB, i.e.; just remove the Bootstrapping capacitor, CB. Now you have taken away the Bootstrapping.

Voltage gain without bootstrap

Vi							Vi, max
Vo							
Av							

To measure Input Impedance Z_i:

1. Connect the circuit as shown below.



2. Set the DRB to minimum (0 Ω). Apply a10 KHz sine wave signal of amplitude 1V (p-p) or any suitable value to get an undistorted output.
3. Measure V_O (p-p). Let V_O = Va (say) with DRB value = 0
4. Increase DRB value in steps till $V_O = V_A/2$. The corresponding DRB value gives Z_i.

5. Repeat the experiment by disconnecting CB, the bootstrapping capacitor.
6. Compare the two input impedance values you have measured.

To measure output impedance, Zo:

1. Connect the circuit as shown in figure

2. Set the DRB to its maximum resistance value. Apply a 10 KHz sine wave of amplitude 1V (p-p) or any suitable value to get undistorted output
3. Measure V_O (p-p), $V_O = V_B$ without DRB connection or DRB value at Max.
4. Decrease DRB value in steps till $V_O = V_B/2$. The corresponding DRB value gives Z_O.
5. In this part of the experiment, it is likely that the o/p wave form may get distorted as the DRB value is decreased. Then, V_I has to be set to a lower value and the steps to be repeated. Note carefully that the answer will be wrong if you take readings with distorted output.
6. Repeat the experiment by disconnecting the Bootstrapping capacitor.

Result:

1. Voltage Gain with Boot Strap. : …….
2. Voltage Gain with Boot Strap. : …….
3. Input Impedance, Zi, with Bootstrap. : …….
4. Input Impedance, Zi, without Bootstrap. : …….
5. Output Impedance, Z0, with Bootstrap. : ……
6. Output Impedance, Z0, without Bootstrap. : …….
7. Current Gain, Ai, With Bootstrap. : ……
8. Current Gain, Ai, Without Bootstrap. : …….

Vi = Zi × Ii, Vo =Zo × Io, Ai = (Io/Ii) = AV × (Zi/Zo)